

AMENDMENTS TO THE CLAIMS

The following list of claims replaces all prior versions, and listings, of claims in the application:

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1-5 (cancelled without prejudice or disclaimer)

6-12 (withdrawn in response to restriction requirement)

13. (amended) A method of resolving B bit long addresses of packets into prefixes of any length up to B by the use of a data structure which comprises a length sorted table Q and a plurality of secondary search units, table Q containing data related to prefixes of length less than not exceeding A, A<B and each secondary search units including tables V and T which are in one-to-one correspondence to one another and each consists of comprising a 2xM memory, M being a positive integer, the method comprising steps of :

(1) indexing table Q by using the first A bits of an address to generate a corresponding prefix of length equal to or less than A, or a pointer to a secondary search unit;

(2) accessing table V of the secondary search unit indicated by the pointer using each successive remaining bit of the address in order;

(3) accessing table T of the secondary search unit at each successive location corresponding to the location of table V accessed in step (2); and

(4) reading a valid data contained at the location in table T, the valid data being a prefix of length more than A.

14. (amended) The method according to claim 13 wherein steps (2)-(4) are performed in one or more for at least two of said addresses in at least two of the secondary search units in parallel.

15. (original) The method according to claim 14, wherein each secondary unit comprises one or more search branches and a pointer to a secondary search unit indicates the identity of the secondary unit and a branch number h so that data relating to two or more

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search branches are interleaved in tables V and T of a secondary unit, the method further comprises a step of accessing table V at a location indicated by the branch number h of the secondary unit identified by the pointer.

16. (original) The method according to claim 15, wherein the step of accessing table V in each identified secondary search unit comprises further steps of:

- (5) accessing table V by using the first bit of the remaining bits of the address at a location identified by branch number h;
- (6) reading table V at the location which indicates a next location of table V;
- (7) continue accessing and reading each successive location using each successive bit of the remaining bits until the Bth bit; and
- (8) continue reading the valid data contained at the location in table T corresponding to the successive locations read in the step (7).

17. (original) The method according to claim 16, comprising further steps of:

- accessing table T at a location corresponding to each successive location accessed in steps (5)-(7);
- recording the data contained at each accessed location of table T; and
- reading the valid data contained at the latest previously accessed location if the last accessed locations contained no valid data.

18. (original) The method according to claim 17, wherein u_j is the j^{th} bit of the B-bit received address, and the address is known to belong to branch h, the steps of accessing and reading table V and T in each secondary search unit are performed as follows to generate a prefix t:

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y=h, t=0  
for 1≤d≤B  
{  
    x=ud ;  
    if (T(x, y) >0) t=T(x, y);}
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y=V(x, y)
if V(x, y) >0, y=V(x, y)

}

A | 19. (original) The method according to claim 18, wherein the step of reading the valid data contained at the location in table T is replaced by steps of:

reading an indicator contained at the location in table T;
accessing a storage device at a location indicated by the indicator; and
reading the valid data contained at the location in the storage device.

20. (original) The method according to claim 19, further comprising a step of:

scrambling all the bits of the addresses to be translated according to a reproducible formula.

21. (original) The method according to claim 20, wherein the reproducible formula is a bit reversal of all the bits in the addresses.

22. (original) The method according to claim 13, wherein length sorted table Q provides an indication of '00' if the address cannot be resolved, "01" if the prefix is found, and "10", if a further search is required in a respective secondary search unit in that a "10" outcome is associated with a branch number.

23. (amended) An apparatus for address translation of a packet, comprising:

a parsing block for receiving the packet and parsing an address of the packet, the each address having length B, B being a positive integer;

~~an indexing block for selecting the first A binary bits of each received addresses, A being a predetermined positive integer and A≤B and for directly accessing a sorted prefix directory by the first A binary bits, A<B, the sorted prefix directory containing translated prefixes of length N equal to or shorter than not exceeding A and data specifying one of a plurality of secondary search units;~~

the plurality of secondary search units each having a plurality of secondary

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memories for searching in parallel through the secondary memories specified by the indexing block for different prefixes of length N longer greater than A;
wherein each secondary memory comprisesing tables V and T containing interleaved tree branches, each of said tree branches corresponding to an entry in said sorted prefix directory, in that tables V and T are in a one-to-one correspondence to one another and each consists of a $2 \times M$ memory, M being a positive integer, table V for accessing successive location for each successive bits above A of the addresses and table T for translated prefixes at a location corresponding to the location accessed in table V.

24. (amended) The apparatus for address translation of a packet according to of claim 23, wherein each prefix of length longer than A belongs to any of prefix trees a specific branch and each secondary memory containing contains prefixes of one or more prefix tree at least one branch.
25. (cancelled, without prejudice or disclaimer to the subject matter contained therein)
26. (amended) The apparatus according to claim 24 25-further comprising a scrambling unit for scrambling the first A bits of the addresses to be translated according to a reproducible formula.
27. (original) The apparatus according to claim 26 wherein the reproducible formula is a bit reversal of the first A bits in the addresses.
28. (original) An address translation apparatus for telecommunications networks in which packets are transported to addresses contained therein, comprising:
 - an address separation unit for separating from a packet an address to be translated;
 - primary translation unit having a primary translation table for translating the address to a prefix, the primary translation table containing prefixes whose widths are less than a predetermined value and locations of branch search data structures in a secondary search

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units; and

a plurality of secondary search units for performing secondary searches in parallel, each secondary unit having the branch search data structure for performing each secondary search and translating the address to a prefix, if the primary translation table indicates the location of a branch search data structure to begin the secondary search.

29. (original) The address translation apparatus according to claim 28, further comprising:
address scrambling unit for scrambling the addresses according to a predetermined reproducible formula.

30. (original) The address translation apparatus for telecommunications networks according to claim 29 further comprising:

a selector for selecting a secondary search unit for performing the secondary search.

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31. (new) The address translation apparatus according to claim 28 wherein said secondary searches are concurrently performed for a number of distinct addresses not exceeding the number of secondary search units in said plurality of secondary search units.

32. (new) A method of translating addresses each comprising a prefix and a remaining part, said prefix having a respective unknown number of bits, the method comprising steps of:

defining an indexing part comprising a predetermined number of bits;
indexing a first memory device containing an indexing table based upon said indexing part;
determining from said indexing a translation code, a first pointer, and a second pointer; and
if said translation code equals a predetermined value,
accessing a secondary memory device from among a plurality of secondary memory

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devices, said secondary memory device corresponding to said first pointer and storing a plurality of prefixes encoded in at least one tree structure; and

performing a tree-search process on one of said at least one tree structures having a root defined by said second pointer, wherein said tree-search process identifies the prefix.

33. (new) The method of claim 32 including a further step of equating the prefix to a word comprising concatenation of said first pointer and said second pointer if said translation code comprises a second predetermined value.

34. (new) The method of claim 32 wherein said steps of indexing, determining, and accessing are executed in a sequential temporal order.

35. (new) The method of claim 34 wherein said tree-search process for one of said addresses is performed concurrently with said tree-search process for at least one other of said addresses in at least two of said secondary memory devices.

36. (new) The method of claim 35 comprising a further step of buffering said second pointer at said secondary memory device if said secondary memory device is in use in said tree-search process for another one of said addresses.

37. (new) A method of resolving addresses comprising steps of:

receiving a first address, said address including a first prefix of unknown length;

indexing, using a fixed part of said first address, an indexing table Q, to read a translation code and data record;

resolving said data record as a translation if said translation code equals a first predetermined value;

resolving said data record to two identifiers if said translation code equals a second predetermined value, a first of said two identifiers indicating a target

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secondary search unit in a plurality of secondary search units and the second of said two identifiers indicating a location in said target secondary search unit; and

resolving said first address as unknown if said translation code equals a third predetermined value.

38. (new) The method of claim 37 wherein said location in said target secondary search unit corresponds to a root of a branch, said branch comprising prefixes having in common said fixed part of said first address.

39. (new) The method of claim 38 wherein said first address, excluding said fixed part of said first address, is further processed by said target secondary search unit to resolve said first address to a translation.

40. (new) The method of claim 39 including a further step of receiving a multiplicity of addresses and for each address in said multiplicity of addresses executing said steps of indexing and resolving to two identifiers.

41. (new) The method of claim 40 wherein at least two of said secondary search units concurrently process at least two addresses in said multiplicity of addresses.

42. (new) The method of claim 41 wherein at least one of said addresses in said multiplicity of addresses is queued in a buffer associated with said target secondary unit.

43. (new) The method of claim 37 wherein said first predetermined value is '01', said second predetermined value is '10', and said third predetermined value is '00'.
